Steps

1. For each block in the block diagram
   1. Write VHDL code
   2. Compile
   3. Generate a block diagram
2. Once all the blocks have been constructed
   1. Implement top\_level design
   2. Make pin assignments
   3. Perform final compilation
   4. Download either .sof or .jic to the FPGA

**Pin Assignments**

* Connect the 50 MHz input to FPGA pin R8
* Connect second\_blink output to any of the eight LEDs
* All other outputs can be assigned to arbitrary pins

**Important Notes**

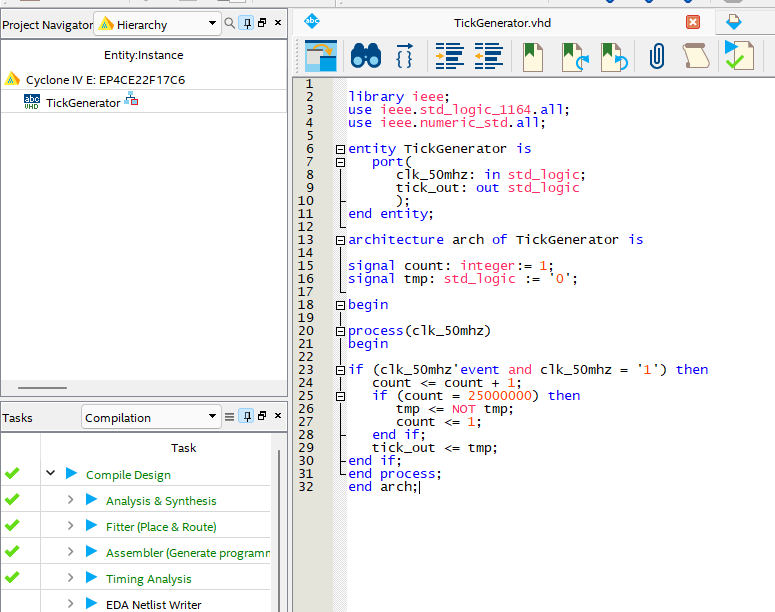
* Clock is not adjustable 🡪 It always starts at 12:00.
* Because the DE0-Nano board does not have a seven segment display or LCD, it is not possible to verify the functionality of this system completely using the DE0-Nano board.
* Writing and compiling code for the top four blocks is worth 80%

**Screenshots of successfully compiled code**

The code and testbenches shown below were compiled using ModelSim which is included with Quartus Lite.

**TickGenerator**

**Code**

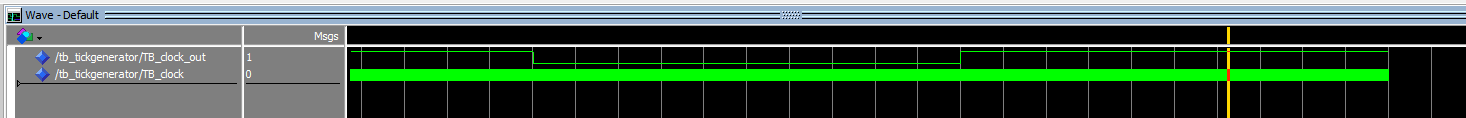
****

**Testbench**

**Text, application

Description automatically generated**

**Testbench output**



**RTL Viewer**

**Diagram

Description automatically generated**

**Second Generator**